AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application.

1 – 6 (CANCELED)

7 (currently amended): A p-n diode comprising:

a silicon carbide substrate;

an n+ region of silicon carbide on said substrate;

an n– voltage blocking region of silicon carbide on said n+ region;

a first p type region of silicon carbide on said n– region;

a p type contact region on said first p type region, said p type contact region having a higher carrier concentration than said first p type region; and

an ohmic contact on said p type contact region;

wherein at least one of said first p type region and said n+ region has a thickness greater than the minority carrier diffusion length in ~~said~~ that respective region.

8 (original): A p-n diode according to Claim 7 wherein said substrate, said voltage blocking region and said p type and n type regions all have the same polytype.

9 (original): A p-n diode according to Claim 8 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

10 (original): A p-n diode according to Claim 7 wherein said n+ region is about 2.5 microns thick and has a carrier concentration of between about 1×10^{18} and 1×10^{19} cm^{-3}.

11 (currently amended): A p-n diode according to ~~Claim 7~~ Claim 10 wherein said n+ region ~~is~~ comprises a layer about 0.5 microns thick ~~and~~ that has a carrier concentration of about 2×10^{18} cm^{-3}.

12 (currently amended): A p-n diode according to Claim 7 wherein said first p type region is greater than about 0.5 microns thick and has a carrier concentration of between about 1×10^{17} and 1×10^{19} cm^{-3}.

13 (original): A p- n diode according to Claim 7 wherein said contact layer has a thickness of about 2 microns and a carrier concentration of about 1×10^{19} cm^{-3}.

14 (currently amended): A p-n diode according to Claim 7 wherein said first p type region has a carrier concentration about 2 orders of magnitude greater than said n– region.

15 (CANCELED)

16 (currently amended): A p-n diode according to ~~Claim 15~~ Claim 7 wherein said contact layer has a carrier concentration of at least about ~~1 x 1019 cm-3~~ 1×10^{19} cm^{-3}, but less than the amount that would result in a decrease in crystal quality that would degrade the performance of the diode, and a thickness of at least about 1000 angstroms.

17 (original): A p-n diode according to Claim 7 wherein said substrate has a carrier concentration of between about 5×10^{18} and 2×10^{19} cm^{-3} and is at least about 125 microns thick.

18 (currently amended): A p-n diode according to Claim 7 wherein:

said first p type region is about 0.5 microns thick and has a carrier concentration of about 1×10^{18} cm^{-3};

said n– region is about 45 microns thick and has a carrier concentration of about 1×10^{15} cm^{-3};

said n+ region is about 0.5 microns thick and has a carrier concentration of about 2×10^{18} cm^{-3};

~~and further comprising a p+ type contact layer between said p type region and said ohmic contact,~~ said p type contact ~~layer~~ region being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3};

and further comprising a n+ type boundary layer between said n– type voltage blocking region and said substrate, said boundary layer being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3}.

19 (original): A p-n diode according to Claim 7 further comprising at least one planar defect, and wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the n+ region or the first p-type region and the remainder of the device.

20 – 48 (CANCELED)

49 (original): A p-n diode according to Claim 10 wherein said n+ region comprises a first n+ region having a thickness of about 0.5 microns and a carrier concentration of about 2E18 cm^{-3} and a second n+ region having a thickness of about 2.0 microns and a carrier concentration of about 1E19 cm^{-3}.

50 – 51 (CANCELED)

52 (New): A p-n diode comprising:

a silicon carbide substrate, said substrate being at least about 125 microns thick and having a carrier concentration of between about 5×10^{18} and 2×10^{19} cm^{-3};

an n+ region of silicon carbide on said substrate;

an n– voltage blocking region of silicon carbide on said n+ region;

a first p type region of silicon carbide on said n– region;

wherein at least one of said first p type region and said n+ region has a thickness greater than the minority carrier diffusion length in that respective region.

53 (New): A p-n diode according to Claim 52 wherein said substrate, said voltage blocking region and said p type and n type regions all have the same polytype.

54 (New): A p-n diode according to Claim 52 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

55 (New): A p-n diode according to Claim 52 wherein said n+ region is about 2.5 microns thick and has a carrier concentration of between about 1×10^{18} and 1×10^{19} cm^{-3}.

56 (New): A p-n diode according to Claim 55 wherein said n+ region comprises a layer about 0.5 microns thick that has a carrier concentration of about 2×10^{18} cm^{-3}.

57 (New): A p-n diode according to Claim 52 wherein said first p type region is greater than about 0.5 microns thick and has a carrier concentration of between about 1×10^{17} and 1×10^{19} cm^{-3}.

58 (New): A p-n diode according to Claim 52 wherein said first p type region includes a contact layer having a thickness of about 2 microns and a carrier concentration of about 1×10^{19} cm^{-3}.

59 (New): A p-n diode according to Claim 52 wherein said first p type region has a carrier concentration about 2 orders of magnitude greater than said n– region.

60 (New): A p-n diode according to Claim 52 and further comprising a p type contact layer on said first p type region and an ohmic contact on said p type contact layer, said p type contact layer having a higher carrier concentration than said p type region.

61 (New): A p-n diode according to Claim 60 wherein said p type contact layer has a carrier concentration of at least about 1×10^{19} cm^{-3}, but less than the amount that would result in a decrease in crystal quality that would degrade the performance of the diode, said p type contact layer further having a thickness of at least about 1000 angstroms.

62 (New): A p-n diode according to Claim 52 wherein:

said first p type region is about 0.5 microns thick and has a carrier concentration of about 1×10^{18} cm^{-3};

said n– region is about 45 microns thick and has a carrier concentration of about 1×10^{15} cm^{-3};

said n+ region is about 0.5 microns thick and has a carrier concentration of about 2×10^{18} cm^{-3};

and further comprising a p+ type contact layer on said n– region and an ohmic contact on said p+ type contact layer, said p+ type contact region being about 2 microns thick and having a carrier concentration of about 1 x 10^{19} cm^{-3};

and further comprising a n+ type boundary layer between said n– voltage blocking region and said substrate, said boundary layer being about 2 microns thick and having a carrier concentration of about 1 x 10^{19} cm^{-3}.

63 (New): A p-n diode according to Claim 52 further comprising at least one planar defect, and wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the n+ region or the p-type region and the remainder of the device.

64 (New): A p-n diode comprising:

a silicon carbide substrate;

an n+ region of silicon carbide on said substrate, said n+ region being about 0.5 microns thick and having a carrier concentration of about 2 x 10^{18} cm^{-3};

an n– voltage blocking region of silicon carbide on said n+ region, said n– voltage blocking region being about 45 microns thick and having a carrier concentration of about 1 x 10^{15} cm^{-3};

a first p type region of silicon carbide on said n– type voltage blocking region, said first p type region being about 0.5 microns thick and having a carrier concentration of about 1 x 10^{18} cm^{-3};

a p+ type contact layer on said first p type region, said p+ type contact layer being about 2 microns thick and having a carrier concentration of about 1 x 10^{19} cm^{-3};

an n+ type boundary layer between said n– type voltage blocking region and said substrate, said boundary layer being about 2 microns thick and having a carrier concentration of about 1 x 10^{19} cm^{-3};

wherein at least one of said first p type region and said n+ region has a thickness greater than the minority carrier diffusion length in that respective region.

65 (New): A p-n diode according to Claim 64 wherein said substrate, said voltage blocking region and said p type and n type regions all have the same polytype.

66 (New): A p-n diode according to Claim 64 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

67 (New): A p-n diode according to Claim 64 wherein said first p type region has a carrier concentration about 2 orders of magnitude greater than said n– region.

68 (New): A p-n diode according to Claim 64 wherein said contact layer has a thickness of at least about 1000 angstroms.

69 (New): A p-n diode according to Claim 64 wherein said substrate has a carrier concentration of between about 5×10^{18} and 2×10^{19} cm^{-3} and is at least about 125 microns thick.

70 (New): A p-n diode according to Claim 64 further comprising at least one planar defect, and wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the n+ region or the p-type region and the remainder of the device.

71 (New): A p-n diode comprising:
a silicon carbide substrate;

an n+ region of silicon carbide on said substrate, said n+ region comprising a first n+ layer having a thickness of about 0.5 microns and a carrier concentration of about 2×10^{18} cm^{-3} and a second n+ layer having a thickness of about 2.0 microns and a carrier concentration of about 1×10^{19} cm^{-3};

an n– voltage blocking region of silicon carbide on said n+ region;

a first p type region of silicon carbide on said n– region;

wherein at least one of said first p type region and said n+ region has a thickness greater than the minority carrier diffusion length in that respective region.

72 (New): A p-n diode according to Claim 71 wherein said substrate, said voltage blocking region and said p type and n type regions all have the same polytype.

73 (New): A p-n diode according to Claim 71 wherein said substrate has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

74 (New): A p-n diode according to Claim 71 wherein said first p type region is greater than about 0.5 microns thick and has a carrier concentration of between about 1×10^{17} and 1×10^{19} cm^{-3}.

75 (New): A p-n diode according to Claim 71 wherein said first p type region includes a contact layer having a thickness of about 2 microns and a carrier concentration of about 1×10^{19} cm^{-3}.

76 (New): A p-n diode according to Claim 71 wherein said first p type region has a carrier concentration about 2 orders of magnitude greater than said n– region.

77 (New): A p-n diode according to Claim 71 and further comprising a p type contact layer on said first p type region and an ohmic contact on said p type contact layer, said p type contact layer having a higher carrier concentration than said first p type region.

78 (New): A p-n diode according to Claim 77 wherein said p type contact layer has a carrier concentration of at least about 1×10^{19} cm^{-3}, but less than the amount that would result in a decrease in crystal quality that would degrade the performance of the diode, said p type contact layer further having a thickness of at least about 1000 angstroms.

79 (New): A p-n diode according to Claim 71 wherein:

said first p type region is about 0.5 microns thick and has a carrier concentration of about 1×10^{18} cm^{-3};

said n– region is about 45 microns thick and has a carrier concentration of about 1×10^{15} cm^{-3};

and further comprising a p+ type contact layer on said n– region and an ohmic contact on said p+ type contact layer, said p+ type contact region being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3};

and further comprising a n+ type boundary layer between said n– voltage blocking region and said substrate, said boundary layer being about 2 microns thick and having a carrier concentration of about 1×10^{19} cm^{-3}.

80 (New): A p-n diode according to Claim 71 further comprising at least one planar defect, and wherein those portions of those stacking faults that grow under forward bias operation are segregated from at least one of the interfaces between the n+ region or the p-type region and the remainder of the device.